

A Shallow Trench Isolation Process For Reduced Junction Leakage

Background Of The Invention

5 Related Patent Applications

Attorney's Docket Number TSMC97-486, Serial Number: _____, Filing Date: _____, "A New Shallow-Trench-Isolation Process", Assigned to the Same Assignee as the present invention.

10 Field of the Invention

The present invention relates to the manufacture of semiconductor devices and more particularly to the manufacture of shallow trench isolation (STI) features of integrated circuits.

15 Description of the Related Art

The structure and function of shallow trench isolation is well known in the art. Shallow trench isolation is commonly used to provide a very high resistance between circuit elements of an integrated circuit to effectively insulate the respective circuit elements from one another.

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Shallow trench isolation is formed by selectively forming recesses or trenches **10** in the surface of the semiconductor substrate **5** as shown in Fig. 1a.

The shallow trenches are filled with an insulating material such as silicon dioxide (SiO_2). Traditionally, the fill layer of silicon dioxide (SiO_2) is formed by chemical vapor deposition (CVD) of ozone assisted tetraethylorthosilane (O_3 - TEOS) or a spun-on-glass (SOG) form of silicon dioxide. The fill oxide layer is planarized by chemical/mechanical planarization (CMP) or chemical etching of the silicon dioxide from the surface of the semiconductor substrate **5**.

Stop layers of silicon nitride (Si_xN_y) **20** and silicon dioxide (SiO_2) **15** are striped to form the transistors of the integrated circuits. Impurity species such as boron (B) and arsenic (As) are diffused into the surface of the semiconductor substrate adjacent to the sidewalls of the trenches **10**. These diffusions form the sources and drains of the transistors of integrated circuits.

The surface of the semiconductor substrate is then etched with dilute hydrofluoric acid (HF) to remove any residual oxides prior to the formation of the contact metallurgy on the sources and drains. The dilute hydrofluoric acid will additionally reduce the thickness of the fill oxide layer in the shallow trench.

Titanium, cobalt, or titanium nitride are alloyed to the surface of the semiconductor substrate at the sources and the drains of the transistors to form

a titanium salicide (TiSi_x) or cobalt salicide (CoSi_x). The reduced thickness of the fill oxide layer causes increased junction leakage.

Further, in p-type sources and drains, the boron (B) implant species will
5 diffuse into the fill oxide layer in the shallow trenches. This will cause a reduction in the carrier concentration in the p-type diffusions forming the sources and drains, thus further increasing the junction leakage of the transistors.

The semiconductor substrate is further processed to complete the
10 metalization and final back end processing to form the integrated circuit.

United States Patent 5,112,772 (Wilson et al.) discloses a method of fabricating a trench structure. The semiconductor substrate has a silicon dioxide layer, a polysilicon layer, and a silicon nitride layer formed on its surface. A
15 trench is formed through the silicon dioxide (SiO_2) layer, the polysilicon layer, and the silicon nitride layer and into the semiconductor substrate. A dielectric liner is formed on the sidewalls of the trench, which is then filled with a trench fill material. Portions of the trench liner above the trench fill material are removed and a conformal layer is then formed on the trench structure. The conformal
20 layer and a portion of the trench fill material are then oxidized.

United States Patent 5,208,179 (Okazawa) teaches a method of fabricating a semiconductor integrated circuit such as a programmable read only

memory (PROM) cell. The method begins with forming a first gate insulating film on a main surface of a semiconductor substrate. A first polysilicon layer, a second gate insulating film, and a second polysilicon layer are then deposited on the surface of the semiconductor substrate. Insulating trenches are then formed by selectively removing the second polysilicon layer, the second gate insulating film, the first polysilicon layer, the first gate insulating film, and the semiconductor substrate. A borophosphosilicate glass (BPSG) film is formed over the entire surface filling the trenches. The BPSG film is selectively removed to leave it only in the trenches. In the prior art of Okazawa, the phosphorus and boron contained in the BPSG evaporated in response to a heat treatment used for forming the gate insulating film. Therefore, a portion of the evaporated phosphorus or boron was taken into the gate insulating film, which degraded the characteristics and the reliability of a PROM cell transistor. The invention grows the BPSG film after the first and second gate insulating film is formed. Hence, phosphorus or boron contained in the BPSG film is not taken into both of the gate insulating films.

United States Patent 5,316,965 (Philipossian et al.) discloses an improved process for planarizing an isolation barrier in the fabrication of an integrated circuit on a semiconductor substrate. The process involves reducing the etch rate of the field oxide independently of the sacrificial oxide layer. The field oxide layer is implanted with nitrogen ions and then thermally annealed resulting in a hardened and densified field oxide. In subsequent operations, a

sacrificial oxide layer is formed on the semiconductor top surface by thermal oxidation. Upon etching with hydrofluoric acid (HF), the etch rate of the hardened field oxide is significantly reduced relative to untreated field oxide. Thus, the exposed hardened field oxide is etched at about the same rate as the sacrificial oxide layer. In the example given, the etch rate of untreated densified TEOS field oxide in 10:1 HF is 6.90 Å/sec, while the etch rate of TEOS field oxide hardened according to the processes of this invention is 5.90 Å/sec. After planarization using the hardened field oxide, depressions in the isolation barrier are eliminated.

United States Patent 5,447,884 (Fahey et al.) relates to a process for forming trench isolation in which the trench is etched in a reactive ion etching process, and lined with a thin liner nitride having a thickness <5 nanometers. A feature of the invention is the use of a pyrogenic oxide anneal (wet oxidation) at a temperature of about 80°C. This anneal densifies the oxide liner as is conventional, but at a much lower temperature than conventional argon annealing.

United States Patent 5,492,858 (Bose et al.) discloses is a method of planarizing the surface of a silicon wafer in integrated circuit manufacture where shallow trench isolation techniques are employed. The etched trenches are first coated with a silicon nitride protective liner before the trenches and active area mesas are conformally coated with a layer of silicon oxide. The conformal oxide

then is steam annealed to densify the conformal oxide, and then the surface of the silicon wafer is etched and polished back down to the tops of the active area mesas, to form a substantially planar surface.

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Summary of the Invention

An object of this invention is to provide a method of forming shallow trench isolation that reduces junction leakage at the boundary of shallow trench isolation and contact metallurgy of adjacent transistors.

Another object of this invention is to provide a method of forming shallow trench isolation that avoids a reduction of carrier concentration in the source and drain region of transistors adjacent to the shallow trench isolation.

To accomplish these and other objects the method to form a shallow trench isolation feature of an integrated circuit on the surface of a semiconductor substrate of this invention begins providing a semiconductor substrate having a surface coated with at least one layer of an insulating material and a plurality of shallow trenches formed in the surface of the semiconductor substrate. A nitrogen doped insulating layer is then grown on the internal surfaces or sidewalls of the shallow trenches. A gap fill insulating layer is deposited upon the surface of the semiconductor substrate to fill the shallow trenches, and the

gap fill insulating layer is planarized to remove excess material of the gap fill insulating layer from the surface of the semiconductor substrate while leaving the gap fill insulating layer within the shallow trenches.

5 The nitrogen doped insulating layer is grown by treating the internal surfaces of the shallow trenches with an oxygen rich atmosphere such as steam (H_2O) and oxygen (O_2) gas followed by a nitrogen compound such as nitrogen gas (N_2), ammonia (NH_3), nitrous oxide (N_2O), and nitric oxide (NO).

10 Alternately, the oxygen rich atmosphere and the nitrogen compound are applied simultaneously to treat the internal surface of the shallow trenches.

15 The treating of the internal surfaces of the shallow trenches with the oxygen rich atmosphere of the shallow trenches is at a temperature from approximately 900°C to approximately 1000°C , at a pressure of from approximately 600 Torr to approximately 760 Torr, for a period of time from 60 minutes to 120 minutes.

20 The treating the internal surfaces of the shallow trenches with the nitrogen compounds is at a temperature of from approximately 900°C to approximately 1000°C at a pressure of from approximately 600 Torr to approximately 760 Torr for a period of time of from approximately 30 minutes to approximately 90 minutes.

The growing the nitrogen doped insulating layer on the internal surfaces of the shallow trenches is alternatively performed by exposing the internal surfaces to a mixture of nitrogen rich and oxygen rich compounds to thermally grow a silicon oxynitride layer on said internal surfaces of the shallow trenches. The mixture of nitrogen rich and oxygen compounds is at a temperature of from approximately 900 °C to approximately 1000 °C, and at a pressure of from approximately 600 Torr to approximately 760 Torr for a period of from approximately 120 minutes to approximately 180 minutes. The mixture nitrogen rich and oxygen rich compounds include nitrogen (N₂) gas, ammonia (NH₃), nitric oxide (NO), and nitrous oxide (N₂O) and oxygen rich compounds are steam (H₂O) and oxygen (O₂).

The nitrogen doped insulating layer is grown to a thickness from approximately 10 nanometers to approximately 30 nanometers.

The gap fill insulating layer is CVD formed silicon oxide or spun-on-glass silicon dioxide. The planarizing is accomplished by chemical/mechanical planarization or by etching the gap fill insulating layer.

Brief Description Of The Drawings

Fig. 1a - 1f are cross sectional diagrams showing the steps of forming a shallow trench isolation of this invention.

Fig. 2 is a flow chart of the method to form a shallow trench isolation of
5 this invention.

Detailed Description Of The Invention

10 Refer now to Figs. 1a - 1f and Fig. 2 for a discussion of the method to form the shallow trench isolation of this invention. The method of this invention begins with providing **100** a semiconductor substrate as shown in Fig. 1a. The semiconductor substrate **5** has a first insulating layer **15** that is usually a silicon oxide (SiO_x) and a second insulating layer **20**. The second insulating layer is
15 conventionally a silicon nitride Si_xN_y layer that will act as a planarization stop in later steps of this method. A trench **10** is formed by selectively etching the first insulating layer **15**, the second insulating layer **20**, and the semiconductor substrate **5**.

20 An insulating liner **25** that is rich in nitrogen is grown **105** on the inner surface or sidewalls of the trench **10** as shown in Fig. 2b. The insulating liner **25** is formed by exposing the internal surfaces or sidewalls of the trenches **10** to an atmosphere that is a mixture of nitrogen (N_2) gas or nitrogen compounds such as

ammonia (NH_3), nitric oxide (NO), and nitrous oxide (N_2O), and oxygen (O) rich compounds such as steam (H_2O) or oxygen (O_2) gas. The pressure of the atmosphere is from 600 Torr to 760 Torr and the temperature is from approximately 900 °C to approximately 1000 °C. The period of time of exposure to the atmosphere is from approximately 120 minutes to approximately 180 minutes or until the insulating liner has achieved a thickness greater than 8 nanometers.

Alternately, the atmosphere is initially is an oxygen rich compound of either steam (H_2O) or oxygen (O_2) gas applied at a temperature of from approximately 900 °C to approximately 1000 °C at a pressure of from approximately 600 Torr to 760 Torr. The period of exposure to the steam (H_2O) or oxygen (O_2) gas is from approximately 60 minutes to approximately 120 minutes. This above described process is equivalent to the conventional thermal oxide growth. The atmosphere of oxygen rich compound of steam (H_2O) or oxygen (O_2) gas is then replaced with an atmosphere of gaseous nitrogen compounds such as nitrogen (N_2) gas, ammonia (NH_3), nitric oxide (NO), and nitrous oxide (N_2O).

The gaseous nitrogen compounds are applied at a temperature of from approximately 900 °C to approximately 1000 °C and at a pressure of from approximately 600 Torr to approximately 760 Torr. The gaseous nitrogen

compounds from approximately 30 minutes to approximately 90 minutes. The insulating layer will have a thickness greater than 10 nanometers.

The insulating liner **25** must be a form of silicon oxynitride ($\text{Si}_x\text{O}_y\text{N}_z$). If the insulating liner **25** were formed as strictly a silicon nitride (Si_xN_y), stresses due to the lattice mismatch of the silicon nitride (Si_xN_y) and the silicon (Si) of the semiconductor substrate **100** easily lead to the formation of defects around the trenches **10**. The above described stresses are typically greater than 5×10^9 dynes/cm² in tension.

The next step is the deposition **110** of the gap fill layer **30** of Fig. 1c on the surface of the semiconductor substrate **5**. The gap fill layer **30** is formed by conventional methods well known in the art. These methods include chemical vapor deposition (CVD) of ozone assisted tetraethylorthosilane (O_3 - TEOS), spun-on-glass (SOG).

The gap fill layer **30** is silicon dioxide (SiO_2) or borophososilicate glass (BPSG).

The gap fill layer **30** is annealed **115** at a temperature of from approximately 800 °C to approximately 1200 °C for a period of time from approximately 60 minutes to approximately 120 minutes. The high temperature anneal causes the gap fill layer to become more dense.

After the high temperature anneal **115**, the surface of the semiconductor substrate **5** is planarized **120** to remove the excess gap fill layer **30** from the surface of the semiconductor substrate as shown in Fig. 1d. The gap fill layer **30** fills the trenches **10** level to the top surface of the semiconductor substrate **5**.

- 5 The planarizing **120** of the gap fill layer **30** is performed by conventional methods of chemical/mechanical planarization (CMP) or by conventional wet etching techniques.

The method continues with conventional formation **130** of the transistors **40** of Fig. 1c on the surface of the semiconductor substrate. The source and drain **35** of the transistor **40** is formed by diffusing an impurity species such as boron (B) into the surface of the semiconductor substrate **5**. As described above boron (B) will diffuse more readily into the gap fill layer **30**. However, the boron (B) will be stopped by the nitrogen (N) present in the insulating liner **25**. The process for the nitrogen (N) stopping the diffusion of the boron (B) into the gap fill layer **30** is similar to that of the process wherein the nitrided gate oxide is used to suppress the penetration of Boron (B) from a heavily doped polycrystalline silicon or amorphous silicon gate through the gate oxide to the silicon semiconductor substrate **5**. This phenomena is well reported in the prior art.

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The carrier concentration of the source and drain **35** at the sidewall of the trench **10** thus will not decrease to unacceptable levels and cause an increase in the junction leakage of the transistor **40**.

5 Subsequent to the formation of the transistor **40**, the surface of the semiconductor substrate **5** in the areas of the source and drain **35** has a dilute solution of hydrofluoric acid applied **140**. The dilute solution of hydrofluoric acid is to remove any residual of the gap fill layer **30** from the surface of the semiconductor substrate **5** in the area of the source and drain **35**. The insulating
10 liner **25** will further act as a stop barrier to prevent further thinning of the gap fill layer **30**, thus preventing increased junction leakage in the transistor **40**.

The contact metallurgy is formed **145** by depositing either titanium (Ti) or cobalt (Co) or cobalt (Co) and an optional titanium nitride (TiN). A rapid thermal
15 anneal (RTA) is performed on the contact metallurgy at a temperature of from approximately 500° C to approximately 800° C for a period of time from 20 seconds to 40 seconds. The contact metallurgy will be selectively etched and a second rapid thermal anneal (RTA) is performed. The second rapid thermal anneal is performed at a temperature of from approximately 650° C to
20 approximately 750° C. The aforementioned process will create a titanium salicide or cobalt salicide at the interface between the contact metallurgy and the source and drain **35**.

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The invention claimed is: